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Attorney Docket No.: 00939H-079800US Client Reference No.: P00H9013/US/kj

Assistant Commissioner for Patents

Washington, D.C. 20231

IN THE UNITED STATES PATENT AND TRADEMARK O

In re application of:

SEONG-HOON LEE

Application No.: TBA

Filed: October 2, 2001

For: DELAY LOCKED LOOP FOR USE

IN SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY

Art Unit:

**TBA** 

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97 an

§1.98

**Assistant Commissioner for Patents** Washington, D.C. 20231

Sir:

The references cited on attached form PTO/SB/08B are being called to the attention of the Examiner. Copies of the references are enclosed. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

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This statement is being filed concurrently with the above-captioned application. Applicant believes that no fee is required for submission of this statement. However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,

Horace H. Ng Reg. No. 39,315

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STAT	EMENT BY APPLICANT	First Named Inventor	Lee, Seong-Hoon	7:
		Group Art Unit		~2
	(use as many sheets as necessary)	Examiner Name		88
Sheet	1 of	Attorney Docket Number	00939H-079810US	

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·-	А	WP 24.5 A250Mb/s/pin 1Gb Double Data Rate SDRAM with a BI-Directional Delay and an Inter-Bank Shared Redundancy Scheme, 1999 IEEE International Solid-State Circuits Conference	
•	В	WP 24.2 A2.5V333Mb/s/pin 1Gb Double Data Rate SDRAM, 1999 IEEE International Solid-State Circuits Conference	
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